



Computer Organization

ECSE324, section 001

April 24th, 2020, 9am

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STUDENT NAME:		McGILL ID:												
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EXAM:	CLOSED BOOK <input type="checkbox"/>	OPEN BOOK <input checked="" type="checkbox"/>
	SINGLE-SIDED <input checked="" type="checkbox"/>	PRINTED ON BOTH SIDES OF THE PAGE <input type="checkbox"/>
	MULTIPLE CHOICE ANSWER SHEETS: YES <input type="checkbox"/> NO <input checked="" type="checkbox"/> <small>NOTE: The Examination Security Monitor Program detects pairs of students with unusually similar answer patterns on multiple-choice exams. Data generated by this program can be used as admissible evidence, either to initiate or corroborate an investigation or a charge of cheating under Section 16 of the Code of Student Conduct and Disciplinary Procedures.</small>	
	ANSWER BOOKLET REQUIRED: YES <input type="checkbox"/>	NO <input checked="" type="checkbox"/>
	EXTRA BOOKLETS PERMITTED: YES <input type="checkbox"/>	NO <input checked="" type="checkbox"/>
	ANSWER ON EXAM: YES <input type="checkbox"/>	NO <input checked="" type="checkbox"/>
SHOULD THE EXAM BE: RETURNED <input checked="" type="checkbox"/> KEPT BY STUDENT <input type="checkbox"/>		
CRIB SHEETS:	PERMITTED <input type="checkbox"/> <u>Specifications:</u> (ex: one 8 1/2X11 handwritten double-sided sheet) NOT PERMITTED <input checked="" type="checkbox"/>	
DICTIONARIES:	TRANSLATION ONLY <input type="checkbox"/> REGULAR <input checked="" type="checkbox"/> NOT PERMITTED <input type="checkbox"/>	
CALCULATORS:	NOT PERMITTED <input type="checkbox"/> PERMITTED (Non-Programmable) <input checked="" type="checkbox"/> PERMITTED (Programmable) <input type="checkbox"/>	
ANY SPECIAL INSTRUCTIONS: e.g. molecular models		

Important information, please read it in full

Communication embargo: Please remember that you are not allowed to communicate (online or offline) with anyone else about the content of this exam **until the end of the exam** (24h after the start time). If anyone tries to get in touch with you during this period to discuss the content of this exam, please report it immediately by email to the instructor (christophe.dubach@mcgill.ca).

Response format: This PDF version is provided as a backup and should only be used in case you encounter issues with the online quiz on mycourses. If you decide to use this PDF for your exam, please return all your answers in a text file (no photo/scan) before the end of the exam. Each answer should be correctly labelled with the proper number from the corresponding question in the PDF. For answers requiring to fill in a table, simply use colons to separate the columns and a new line to separate the rows. For instance,

1	2	3
4	5	6

is written as:

1, 2, 3
4, 5, 6

Filename: The filename should be exactly:

McGillid_Firstname_Lastname.txt

where you replace Firstname, Lastname and McGillid with your specific information.

Email content: The text file should be sent by email as an **attachment** to the instructor (christophe.dubach@mcgill.ca) with an explanation as to why it is not possible for you to complete the quiz on mycourses. Please note that if you do send your responses by email, we will not look at any answers you may have entered on the online quiz.

In addition, please make sure to read and copy/paste the following text into your email.

By submitting this work, I certify that the work represents solely my own efforts. I confirm that I understand the meaning and consequences of cheating, plagiarism and other academic offences under the [Code of Student Conduct and Disciplinary Procedures](#), and am aware of my responsibilities under the [Student Assessment Policy](#).

1) General knowledge**[total 16 points]**

Short questions, [**1 point**] each. For multiple choice questions, circle your choice. If more than one is circled, you will get zero for that question.

1.1) Given a byte-addressable memory and a 24-bit address space, the maximum capacity of the memory is:

a)	b)	c)	d)	e)
4MB	16MB	4GB	16GB	None of these

1.2) Consider a machine with a memory alignment of 8 bytes. Which addresses are valid to use to access a half-word?

a)	b)	c)	d)	e)
2	4	6	All of these	None of these

1.3) Which register contains the address of an instruction?

a)	b)	c)	d)	e)
CPSR	IR	PC	SP	None of these

1.4) Assuming an 8 bit processor and the content of R1 is 00110011. The content of R2 after executing `ASR R2, R1, #2` is

a)	b)	c)	d)	e)
00110011	11001100	00000011	10001100	None of these

1.5) Which instruction might modify the CPSR (Current Program Status Register)?

a)	b)	c)	d)	e)
TST	CMP	ADDS	All of these	None of these

1.6) Order these components in the order they are usually run:

Loader, Linker, Assembler

1.7) The KIN status flag in the keyboard status register indicates whether an input is ready to be read by the CPU. Assuming that this register is memory mapped, which instruction would you use to check the value of KIN?

a)	b)	c)	d)	e)
TST	CMP	SUB	OR	None of these

1.8) In general, an interruption service routine can:

a)	be executed at any time
b)	disable interrupts
c)	be interrupted
d)	All of these
e)	None of these

1.9) In the context of I/O buses, tri-state buffers are used:

a)	to connect a single device at a time to the bus
b)	to arbitrate between different bus masters
c)	exclusively by asynchronous buses
d)	All of these
e)	None of these

1.10) From the CPU point of view, a DMA controller:

a)	is just another I/O device
b)	keeps the CPU free to run other instructions during data transfer
c)	wakes up the CPU with an interrupt once the transfer is finished
d)	All of these
e)	None of these

Short questions, [**2 points**] each.

1.11) Explain in 2-3 sentences, and **in your own words**, how a DMA controller maximizes data throughput on a PCI bus and which feature does it rely on to achieve this.

1.12) Explain in 2-3 sentences, and **in your own words**, why are serial links more suitable for longer distances and less expensive.

1.13) Explain in 2-3 sentences, and **in your own words**, why some CISC-processors use an interconnect network between the different hardware components (e.g. ALU, Register File, Memory interface, ...) while RISC machines do not need an interconnect network.

2) Assembly

[total 16 points]

Assume an 8-bit processor with a byte-addressable memory and with the following set of instructions together with their semantic and bit encoding.

MOV Rd, #imm // Rd ← imm (immediate value)

0	Rd : 2 bits	imm : 5 bits
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BLT Rs1, Rs2, Raddr // branch to [Raddr] if [RS1 < Rs2]

1	0	Rs1 : 2 bits	Rs2: 2 bits	Raddr: 2 bits
---	---	--------------	-------------	---------------

LD Rd, Raddr // Rd ← [MEM[Raddr]]

1	1	0	0	Rd : 2 bits	Raddr : 2 bits
---	---	---	---	-------------	----------------

ST Rs, Raddr // MEM[Raddr] ← [Rs]

1	1	0	1	Rd : 2 bits	Raddr : 2 bits
---	---	---	---	-------------	----------------

ADD Rd, Rs1 // Rd ← [Rd] + [Rs1]

1	1	1	0	Rd : 2 bits	Rs1: 2 bits
---	---	---	---	-------------	-------------

MUL Rd, Rs1 // Rd ← [Rd] * [Rs1]

1	1	1	1	Rd : 2 bits	Rs1: 2 bits
---	---	---	---	-------------	-------------

We will also assume the following encoding for registers:

R0 = 00, R1 = 01, R2 = 10 and R3 = 11.

Consider the following program.

VEC:	.byte	1,2,3,4,5
	MOV R0,	=VEC
	MOV R1,	#1
	MOV R3,	#3
LOOP:	LD R2,	R0
	ADD R2,	R1
	ST R2,	R0
	ADD R0,	R1
	MOV R2,	=LOOP
	ADD R2,	R3
	BLT R0,	R3, R2

2.1) Given the binary encoding specification above, complete the symbol table below for the program given. Please note that some rows might be not be used in the table. Remember, this is an 8-bit processor.

[2 points]

Symbol Name	Symbol Value

2.2) Given the binary encoding specification above, complete the table below for all memory addresses listed. Op Code/Data should be expressed in binary. If the Op Code / Data is undefined, please state so.

[6 points]

Memory Address	Op Code / Data
0x00	
0x01	
0x02	
0x03	
0x04	
0x05	
0x06	
0x07	
0x08	
0x09	
0x0a	
0x0b	
0x0c	
0x0d	
0x0e	
0x0f	

2.3) What is the content of the memory for the vector Vec at the end of the execution? **[2 points]**

VEC =

--	--	--	--	--

2.4) Using a combination of instructions from the set given above, implement the following pseudo-instruction: **[3 points]**

B Raddr // branch to [Raddr]

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2.5) Using a combination of instructions from the set given above, implement the following pseudo-instruction: **[3 points]**

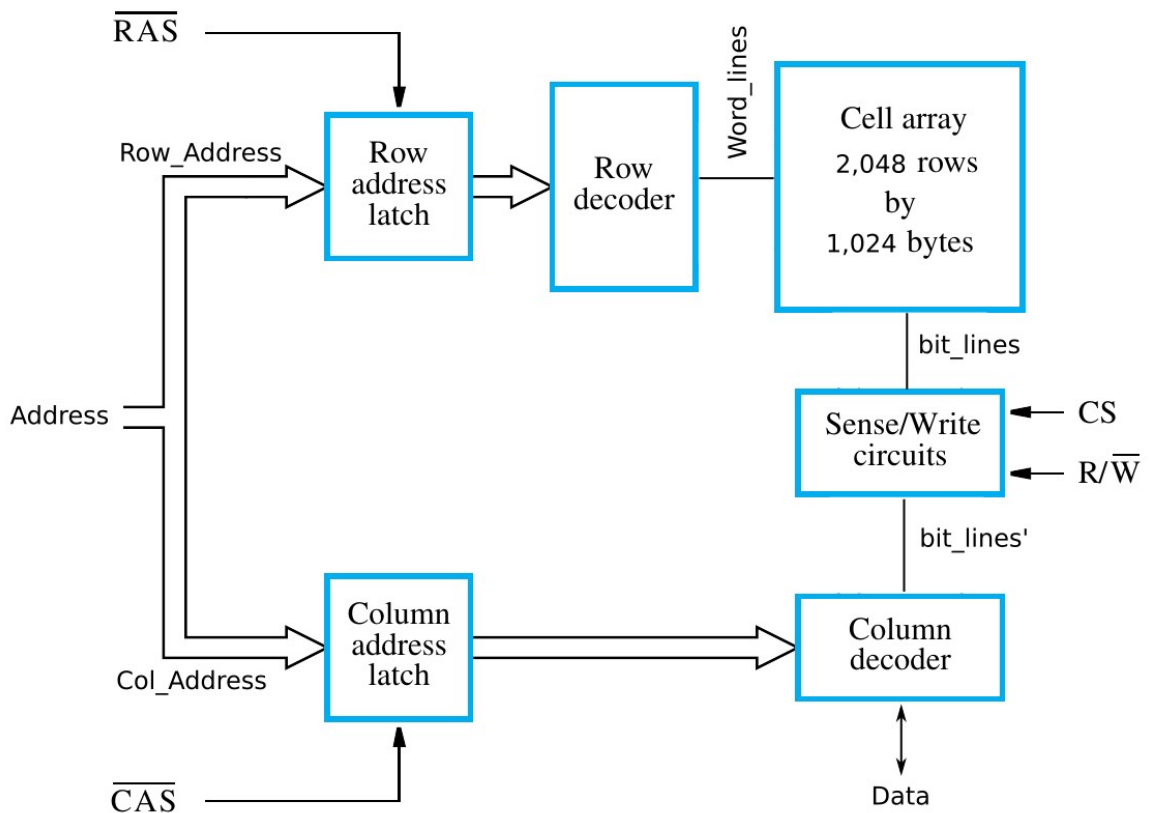
BEQ Rs1, Rs2, Raddr // branch to [Raddr] if [RS1] == [Rs2]

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3) Memory

[total 16 points]

Here is the internal organization of a 32M x 16 asynchronous dynamic memory chip (DRAM).



3.1) Assume the Data signal is 4 bits wide. Indicate what is the minimum width required for each signal below (number of bits). [7 points]

Signal	Number of bits
Address	
Row_address	
Col_address	
Word_lines	
bit_lines	
bit_lines'	
$\overline{\text{CAS}}$	

3.2) Indicate the direction of the following signals (using a combination of East,West,South,North). For instance, the direction of Address is East while the direction for Data is North&South. **[3 points]**

Signal	Direction
Word_lines	
bit_lines	
bit_lines'	

3.3) You are being tasked with designing the control logic to refresh the DRAM above. Assume the Sense/Write circuits has a latch to store a row and that the control logic has direct access to the signals below to perform its task. Which of these signals **are not** needed by the control logic?

[3 points]

address

$\overline{\text{CAS}}$

$\overline{\text{RAS}}$

Data

CS

$\overline{\text{R/W}}$

3.4) Explain in 2-3 sentences, and **in your own words**, what is the advantage of having a latch to store a row and how is this feature called?

[3 points]

4) Cache

[total 16 points]

Consider the following ARM assembly program. The first column corresponds to the address (in decimal) where each data/instruction is stored in memory. The second column contains assembly labels while the third column contains assembly instructions or directives. The last column contains, for each instruction, it's representation in hexadecimal.

Address	Label	Instruction/Directive	Encoding
00	VEC:	.word 0,1,2,3,4,5,6,7	
32	start:	LDR R0, =VEC	0x e59f 0014
36		MOV R1, #0	0x e3a0 1000
40	loop:	LDR R2, [R0,#4]!	0x e5b0 2004
44		ADD R1, R1, #1	0x e281 1001
48		CMP R1, #8	0x e351 0008
52		BLT loop	0x baff fffb
56		B start	0x eaff fff8

Consider the following cache configuration:

- 2-way set-associative
- Block size is 4 bytes
- Cache size is 32 bytes
- Least-recently-used replacement policy

4.1) Consider a dedicated first level (L1) data cache (only data from load or store operations are cached). [total 8 points]

4.1.1) What is the content of set 0 of the cache (show both ways) after instruction at address **56 (B start)** executes for the first time?

[2 points]

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4.1.2) What is the content of set 0 of the cache (show both ways) after instruction at address **56 (B start)** executes for the second time?

[2 points]

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4.1.3) Assuming instruction at address **56 (B start)** has executed 100 times, what is the total number of misses? **[2 points]**

4.1.4) Assuming instruction at address **56 (B start)** has executed 100 times, what is the cache miss rate in percentage? **[2 points]**

4.5) Now, consider a first level (L1) unified cache. A unified cache can store both instructions and data without discrimination. Assume that right before an instruction executes, the instruction is loaded from memory into the cache if not already present. **[total 8 points]**

4.5.1) What is the content of set 0 of the cache (show both ways) after instruction at address **52 (BLT loop)** executes for the first time? **[2 points]**

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4.5.2) What is the content of set 0 of the cache (show both ways) after instruction at address **52 (BLT loop)** executes for the second time? **[2 points]**

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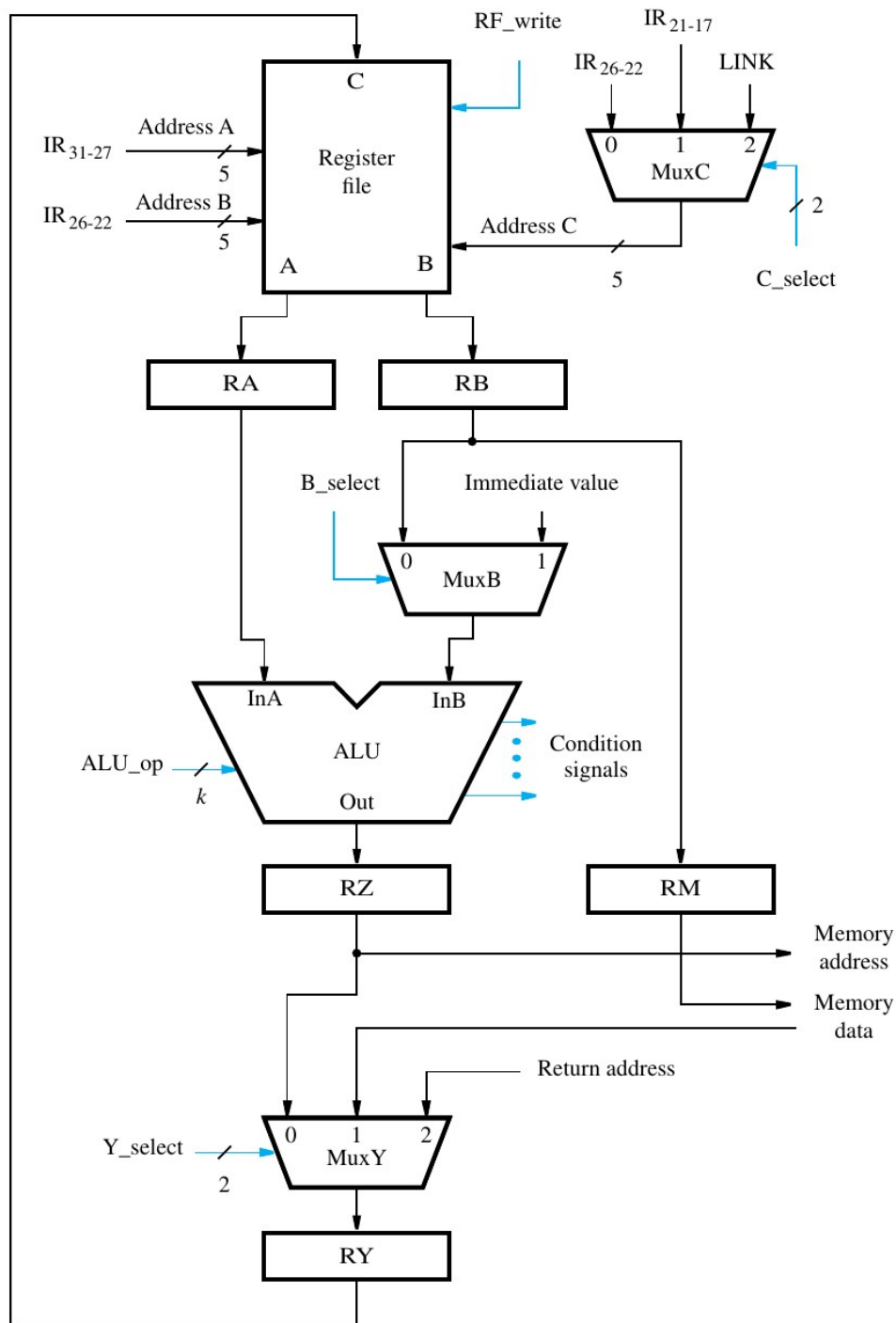
4.5.3) When instruction at address **56 (B start)** is reached for the first time, how many hits in the unified cache? **[2 points]**

4.5.4) When instruction at address **56 (B start)** is reached for the first time, how many misses in the unified cache? **[2 points]**

5) CPU

[total 16 points]

The datapath and control signals of a CPU are given below.



5.1) Assuming you are dealing with an ARM machine, where are the condition signals connected to? [2 points]

5.2) Explain in 2-3 sentences, and **in your own words**, why the Return address is an input to the MuxY multiplexer and why is LINK an input to the MuxC mutiplier. *Hint: think of an instruction that uses these two signals and include this in your explanation.* **[3 points]**

5.3) Given the following instruction, **ADD R1, R2, #4**, what is the content of the following signals at the different stages?

Assume that this is the only instruction being executed by the processor. If the signal is unknown or not relevant for that stage, leave it empty. For the register file addresses, use the register name directly (e.g. R1).

[11 points]

	Stage 2	Stage 3	Stage 4	Stage 5
Address A				
Address B				
Address C				
RF_Write				
C_select				
B_select				
Y_select				