McGill University
Department of Electrical and Computer Engineering

ECSE 324 Final Exam Fall 2020

Name: ____

ID:

Open Book Exam.

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Part D ____________/10

TOTAL 56

Important information, please read it in full

Communication embargo: Please note that you are not allowed to communicate (online or offline) with anyone else about the content of this exam **until the end of the exam** (72h after the start time). If anyone tries to get in touch with you during this period to discuss the content of this exam, please report it immediately by email to the instructor (chrisotphe.dubach@mcgill.ca).

Forbidden to copy/paste: Although it is an open book exam, all your answers should be you own and you are not allowed to use answers from other places directly. For instance, if you find an answer to a question somewhere online, or in a book, it is not acceptable to take that answer and put it in your exam directly, even if you modify the answer slightly. You must write your own answer from scratch.

By submitting this work, I certify that the work represents solely my own efforts. I confirm that I understand the meaning and consequences of cheating, plagiarism and other academic offences under the Code of Student Conduct and Disciplinary Procedures, and am aware of my responsibilities under the Student Assessment Policy.

A) General knowledge [16 points]

Short questions, **[1 point]** each. If more than one answer is selected, you will get zero for that question.

1. The following ARM instruction, LDRB R1, [R3, #4]! updates:

a)	b)	c)	d)	e)
LR	R1 & R3	only R1	only R3	None of These

2. The ARM CPSR contains:

a)	b)	c)	d)	e)
The S bit	The overflow condition code flag	A branch instruction	All of These	None of These

3. The condition field in an ARM instruction is used to determine whether the instruction will actually execute based on the content of:

a)	b)	c)	d)	e)
LR	CPSR	PC	SP	R0

4. On a 32-bit little-endian system, the word of data ABCDEF01 (in hexadecimal) is stored in memory as:

a)	b)	c)	d)	e)
10FEDCBA	ABCDEF01	BADCFE10	01EFCDAB	None of These

5. In the assembler, the content of the symbol table:

a)	b)	c)	d)	e)
Can be determined in a single pass	Requires two passes to be computed	Contains instructions	Contains a map of object files	None of These

6. The Loader is responsible for:

a)	b)	c)	d)	e)
Jumping to start address of program	Computing the symbol table	Moving memory pages to disk	Compiling the program into assembly	None of These

0.1 7. Which instruction can be used to read a memory mapped I/O register?

a)	b)	c)	d)	e)
ADD	LDR	STR	TST	BEQ

8. Polling is achieved by continuously:

a)	b)	c)	d)	e)
Reading the I/O device STATUS register	Reading the I/O device DATA register	Writing into the I/O device STATUS register	Writing into the I/O device DATA register	Raising an exception

9. Tri-state buffers are used to:

a)	b)	c)	d)	e)
Connect multiple devices to the same bus	Implement an arbiter	Buffer data coming over a serial link	All of these	None of These

10. DMA is used for:

a)	b)	c)	d)	e)
Arbitration between different bus master	Freeing up memory when a program has finished running	Avoiding stall in the CPU pipeline	All of These	None of These

11. Consider a write-back cache, what happens during a write miss:

a)	b)	c)	d)	e)
Data is read from the main memory	Data is written into the main memory	The cache is fully flushed	All of These	None of These

12. In a system that supports virtual memory:

a)	b)	c)	d)	e)
The program counter register contains a virtual address	The tags in the cache represent bits of the physical addresses	The content of the stack pointer register is a virtual address	All of These	None of These

13. In a system that supports virtual memory with a TLB, when a page fault occurs:

a)	b)	c)	d)	e)
The TLB is updated	Data is read from the disk and placed in memory	A page from memory may be moved to disk	All of These	None of These

14. Assuming a five-stage classical RISC pipeline, how many write ports in the register files are required to support this ARM instruction: LDR R0, [R1, #8]!

a)	b)	c)	d)	e)
1	2	3	4	None of These

15. On an ARM processor, the condition signals coming out of the ALU are connected to the:

a)	b)	c)	d)	e)
IR	CPSR	PC	Processor-memory interface	None of These

16. Assuming a 32-bit fixed point representation with 8 bits for the fractional part. What is the smallest non-zero positive value that is possible to represent?

a)	b)	c)	d)	e)
1	2^-7	2^-8	2^-24	None of These

B) Problem analysis: Memory [10 points]

We want to design a multi-chip memory that can store 512K (2^19) rows of 16 bits of data using 64K x 8 RAM chips (total 512K bits per chip). Each chip has a input address signal, an input chip-select signal, and an input/output data signal.

17. How many bits of address are required for this entire multi-chip memory?
[2pt]

18. How many bits are required for the address signal connected to each individual chip? **[2pt]**

19. **[6pt]**

Using a 2-D organization, draw a block diagram (similar to slide 27 of the memory lecture) to show how this multi-chip memory can be organized. In particular, show how each bit of the address lines and data lines are connected to the memory chips, and the direction of each wire. Also show how the chip-select signals are connected (using a decoder if required).

C) Problem analysis: Caches [10 points]

For this problem, assume a byte addressable memory with a 32-bit address space, and a cache with the following configuration:

- 2 ways set associative cache
- cache line size of 4B (cache line is also known as cache block)
- total size of 4 KB

20. How many sets are in this cache? **[2pt]**

21. How many bits of the address are used to select a byte in a cache line? **[2pt]**

22. How many bits are required for the tag? **[2pt]**

23. Assume the following trace of memory operations, each loading 32bits (4 Bytes) of data from memory into the cache:

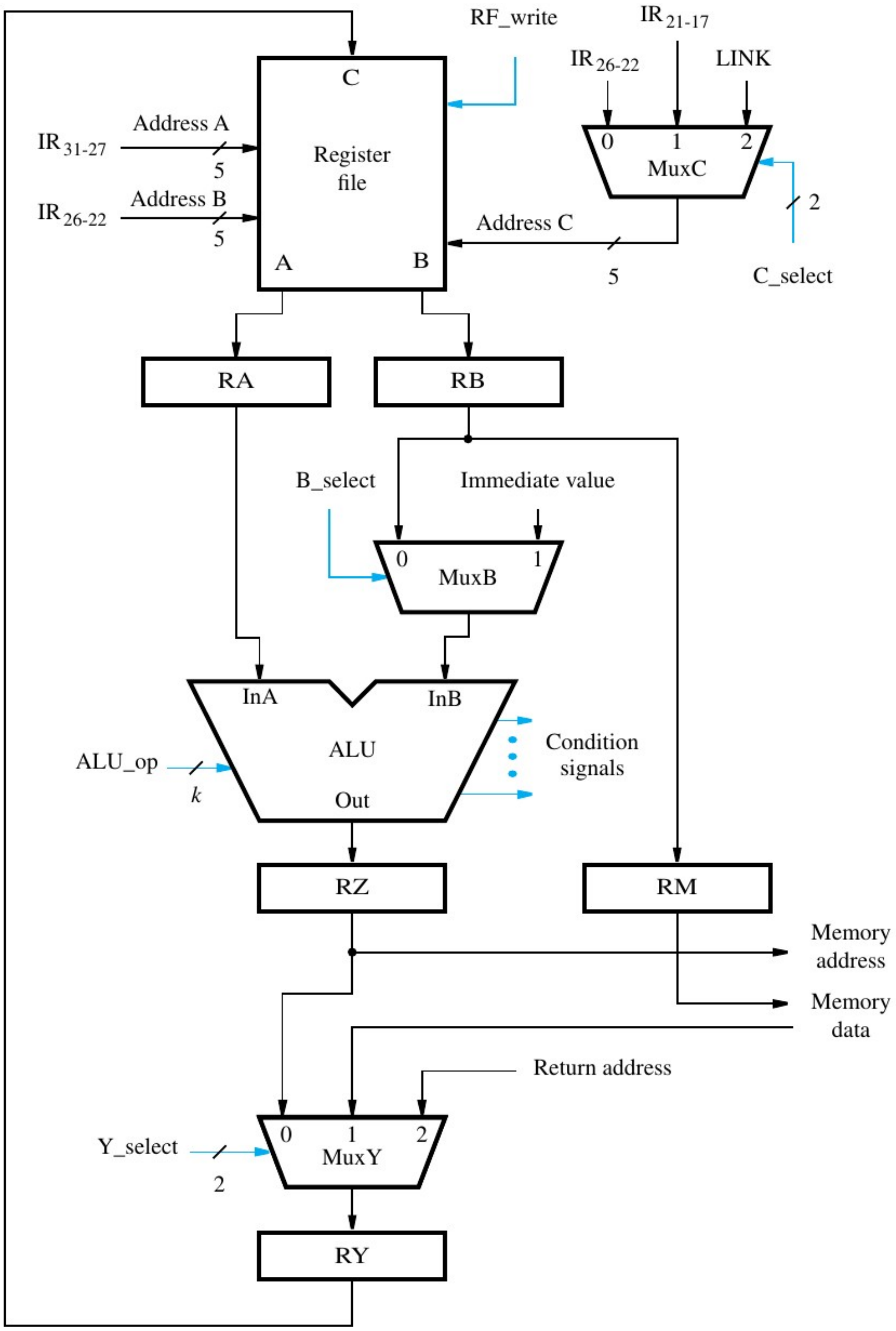
LOAD 0x00004000 // load data at memory address 0x00004000 into the cache
LOAD 0x00004004
LOAD 0x00004008
LOAD 0x0000400C
LOAD 0x00004000
LOAD 0x00004004
LOAD 0x00004008
LOAD 0x0000400C

How many hits in the cache (assuming the cache is empty at the start)? **[2pt]**

24. Now assume the cache line size is 16B and the other parameters remain unchanged (2-way, 4KB total size). How many hits in the cache for the same memory trace given above (assuming the cache is empty at the start)? **[2pt]**

D) Problem Analysis: Processor [10 points]

The datapath and control signals of a 5-stage **pipelined** RISC CPU are given below.



For the following question, consider the following sequence of assembly instructions:

```
ADD     R1, R3, R5
MUL     R3, R4, #4
STR     R3, [R1,#4]
```

[2pt]

25. Highlight any data dependencies in the three instructions above (indicate which instruction depends on which and which register is involved for each dependency).

[6pt]

26. What is the value of each control signal below for clock cycle 1 to 10?

Assume that the store operation in the memory stage only takes a single cycle to complete. Also assume that the first clock cycle corresponds to the fetch stage of the first instruction. If the signal is unknown or not relevant for that stage, leave it empty. For the register file addresses, use the register name directly (e.g. R1), for the ALU operation, use the opcode (e.g. ADD).

Cycle:	1	2	3	4	5	6	7	8	9	10
Address A										
Address B										
Address C										
RF_Write										
B_select										
Y_select										
ALU_op										

27. The sequence of instructions above requires a total of 10 clock cycle to fully execute (i.e. go through all stages for each instructions) due to a data dependency. Explain in your own word and show how you would modify the datapath above to prevent the stall and enable the full execution of these three instructions in only 7 cycles. **[2pt]**

E) Problem analysis: Arithmetic [10 points]

Assume the IEEE 754 Floating point standard for single precision (32bit).

28. Consider two consecutive powers of two numbers, 2^i and 2^(i+1), that are representable as normalized floating point numbers. How many unique floating point values exist between two such consecutive powers of two (excluding the highest power)? In other words, how many different floating point values f satisfy 2^i <= f < 2^(i+1)? **[2pt]**

29. Describes, step by step (bullet point style), a process to convert a floating point number to the nearest integer in two's complement representation (32 bits).

For this question, we will assume that we only deal with normalized numbers (i.e. e! =00000000), we don't have to deal with special values (i.e. e!=11111111), and that the floating point number is within the range of values representable by an integer.

Furthermore, to simplify the problem, we will assume that we round towards the smallest absolute integer:

floatToInteger(10.01) = 10
floatToInteger(10.11) = 10
floatToInteger(-10.11) = -10

[5pt]

30. Design a circuit that achieves the process described in the previous question. You should build your circuit out of coarse-grained components such as: add/subtract units, absolute units, multiplexers, left/right shifters. For each component, make sure to show how the data flows and where the control bits are connected explicitly.

[3pt]